IN THE CLAIMS:

1. (Currently amended) A multiple-processor system comprising:

a) A plurality of nodes, each node including one or more processors, a shared memory space, portions of which are resident in respective nodes;

b) an inter-node switch unit linking each of the nodes with other nodes to provide the communication among the nodes, the switch unit serving as an ordering ~~ordinary~~ point for memory reference requests; said switch unit comprising:

1. a plurality of input switches, each of which (a) is connected to receive messages transmitted by a different group of processors; (b) and is configured to transmit messages selectively over a plurality of inter-switch output terminals, and (c) issues atomic messages corresponding to each memory reference request from a node connected to that switch; and

2. a plurality of output switches, each of which: (a) is connected to receive messages from an inter-switch output terminal of each of the input switches ~~and~~, (b) selectively transmits outputs to a group of nodes connected to that switch; and (c) follows the same ordering rule relative to input switches from which the messages are received simultaneously.

2. (Original) The system defined in claim 1 in which all of said input switches operate in synchronism with the same clock.

3. (Original) The system defined in claim 1 in which all of said output switches operate in synchronism with the same clock.

4. (Currently amended) The system defined in claim 1 in which

A. a source node containing a processor that issues a memory write request transmits the request to a home node of the memory location involved in the request;

B. the home node transmits to the input switch connected thereto a message packet identifying (1) the memory location, (2), the processors having copies of contents of the memory location and (3) the processor that is the source of the request; and

C. The input switch transmits (1) messages identifying the memory location to the processors identified in the message from the home node, and (2) acknowledgement message to the home node, the messages from the switch to the source node and the home node being transmitted no earlier than any of the other messages.

5. (New) The system defined in claim 2 in which all of said output switches operate in synchronism with the same clock.

6. (New) The system defined in claim 1 wherein:

the connections between the input switches and the output switches define paths, and

all paths maintain message order.

7. (New) The system defined in claim 1 wherein one or more of the atomic messages corresponding to a memory reference request include a commit-signal structure indicating apparent completion of the memory reference request rather than actual completion of the request.

8. (New) The system defined in claim 1 wherein the inter-node switch is configured to impose a weak-ordering consistency mode wherein inter-reference ordering is imposed by a memory barrier (MB) instruction inserted between sets of memory reference requests.